Notice of Allowability	Application No.	Applicant(s)	
	10/023,819	CHANDRAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE under 37 CFR 1.114 and Petition under 37 CFR 1.313(c)(2) filed 22 Oct 2004*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☒ The drawings filed on *21 December 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1004//22 Oct 2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on October 22, 2004 has been entered.

Allowable Subject Matter

2. Claims 1-29 have been allowed.

3. The following is an examiner's statement of reasons for allowance:

As to Claims 1-9, patentability resides in *thermally expanding each of the semiconductor chip and substrate substantially the same amount in a direction along surfaces thereof to be joined by soldering*, in combination with the other limitations of base Claim 1.

As to Claims 10-13, patentability resides in *thermally expanding each of the first and second members substantially the same amount in a direction along surfaces thereof to be joined*, in combination with the other limitations of base Claim 10.

As to Claims 14-16, 20, 21 and 22-24, 28, 29, patentability resides in the limitation wherein ***the magnitude of the elongation mismatches and the stresses***

induced thereby *in the electronic assembly are less than one-half that expected based upon cooling the substrate and semiconductor chip* ***from the solder solidification temperature to room temperature following soldering of the soldered joints***, in combination with the other limitations of base Claims 14 and 22, respectively.

As to Claims 17-19 and 25-27, patentability resides in the limitation wherein *the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements*, in combination the other limitations of base Claims 17 and 25, respectively.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 1-16, 20, 21, 17-19, 22-24, 28, 29 and 25-27 of the instant allowed Application will be renumbered as Claims 1-29, respectively, for publication in the issued patent.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Barton (US 5,308,980) discloses a "sandwich" structure comprising a thinned silicon chip 12 on a substrate 11 (Figs. 4 and 9d), the thicknesses of the chip and substrate and material of the substrate chosen to match or approximate the CTE of the

detector device 13 to which the system of chip and substrate is coupled (Figs. 3a,b and 9e) by means of indium bumps 18 and epoxy resin bonding material (col.6: 7-10). By matching the CTE of the chip 12 and substrate 11 assembly with the CTE of the detector 13, the coupled package of elements 11, 12 and 13 exhibits small magnitude of elongation mismatches and stresses induced thereby during the cooling of the package from room temperature (300K) to cryogenic temperatures (e.g., 77K) during package operation. Barton does not teach or suggest any reduction in magnitude of the elongation mismatches and the stresses induced thereby due to the interconnection bonding process involving indium bumps 18 and epoxy resin bonding material over temperatures ranging from an elevated bonding temperature down to room temperature.

b) The articles of Hong, Karim et al., Wang et al. and Xiao et al. (submitted with Applicant's IDS filed October 22, 2004 as Paper No. 1004) disclose special solder compositions, bump materials and/or bump shapes that are shown to be reliable under thermal fatigue induced stresses. These metallurgical structures compensate for, but do not reduce, and are not taught as reducing, the magnitude of thermally induced elongation mismatches between chip and substrate.

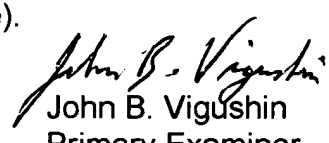
c) Bolduc (US 6,402,012 B1; submitted with Applicant's IDS filed October 22, 2004 as Paper No. 1004) discloses controlling the standoff height of solder-jetted bumps to relieve thermally induced stresses (col.2: 18-26) but does not teach reduction in the magnitude of thermally induced elongation mismatches between chip and substrate.

d) Soga (US 6,555,052 B2; submitted with Applicant's IDS filed October 22, 2004 as Paper No. 1004) discloses bump material having tensile strength, superior elongation and low elasticity (col.12: 50-59) in order to reliably withstand thermal and mechanical shock forces (col.7: 52-col.8: 13; col.9: 20-39 and 56-64) but does not teach reduction in the magnitude of thermally induced elongation mismatches between chip and substrate.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
April 08, 2005